

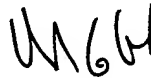
REMARKS

These remarks are in response to the to the final Official Action mailed on September 5, 2003. The Office Action allowed claims 35, 36, 38-40, 45, and 48-51 and rejected claim 46 under 35 U.S.C. 112, with claim 47 also rejected under 35 U.S.C. 112 as it depends upon claim 46.

Claim 46 has been amended to read "rewriting ~~the~~ data content previously stored in said plurality of memory cells" to make clear the antecedent basis and make clear that it is data previously stored in the memory cells that is being referred to. It is believed that claim 46 and claim 47 are now therefore allowable. (The Applicants are unclear as to what the Office Action is referring to when it states that "it is not clear as to whether 'rewriting data content' means 'generating another/other read voltage/s' or 'data that is not identical to read voltage/s' since the various read voltages of claim 45 are part of a sensing or read process, whereas the "rewriting" of claim 46 is a programming or writing process.)

It is respectfully requested that the present amendment be entered and that the Office Action's rejection of claims 46 and 47 be reconsidered.

Respectfully submitted,



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APPENDIX

Pending claims

35. A memory device comprising:
a plurality of memory cells, each of which is readable by application of a read voltage; and

means for determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results.

36.(Previously Amended) The memory device of claim 35, wherein a group of the plurality of memory cells are arranged in a row that includes the first cell, the memory device further comprising means for rewriting a previously stored value into each of the group of memory cells when the means for determining determines that the first cell has a degraded state.

(Claim 37 has been cancelled.)

38. The memory device of claim 35, wherein:
a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a write is performed on the group of memory cells.

39. The memory device of claim 35, wherein:
a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a read is performed on the group of memory cells.

40. The memory device of claim 35, wherein the terminal of the first cell is a control gate terminal of the first cell.

(Claims 41-44 have been cancelled.)

45.(Previously Amended) A method of operating a memory device having a plurality of memory cells, comprising:

- generating a first read voltage;
- applying said first read voltage to a terminal of a first cell of the plurality of memory cells;
- generating a first read result in response to said applying said first read voltage;
- generating a second read voltage;
- applying said second read voltage to said terminal of said first cell;
- generating a second read result in response to said applying said second read voltage; and
- determining from said first and second read results whether data storage of the memory device is deteriorated.

46.(Currently Amended) The method of claim 45, further comprising:

- rewriting data content previously stored in said plurality of memory cells in response to determining from said first and second read results that the data storage of the memory device is deteriorated.

47.(Previously Amended) The method of claim 46, wherein the data content rewritten into said plurality of memory cells in said rewriting are determined based on error correction code (ECC).

48. The method of claim 45, wherein said method is part of a programming process.

49. The method of claim 45, wherein said method is part of a reading process.

50. The method of claim 45, wherein said memory cells are multi-state memory cells.

51. The method of claim 45, wherein said memory cells are floating gate transistors and said terminal is a control gate.